## CLAIMS

1. A circuit for controlling a memory including at least two areas to which access cannot be had simultaneously, the circuit including:

first means for storing a series of read and/or write instructions separately for each of said areas,

second means for detecting that a first instruction intended for a first area is a predetermined instruction to be followed by a period during which the first area can receive no other instruction, and

third means for, during said period, providing instructions to another memory area.

2. The circuit of claim 1, for controlling a memory, each of the memory areas of which is accessible via a specific cache.

3. The circuit of claim 1, further including fourth means for receiving read and/or write requests and for writing each of them in the form of a series of instructions into the first means, each series of instructions including a predetermined number of data.

4. The circuit of claim 3, wherein said predetermined number of data of a series of instructions especially includes an indication of the priority order existing between each series of instructions stored in the first means.

5. The circuit of claim 3, wherein said predetermined number of data of a series of instructions includes an indication of whether the series of instructions aims at a reading from or at a writing into the memory.

6. The circuit of claim 3, wherein said predetermined number of data of a series of instructions includes the addresses for which said series of instructions is intended.

7. The circuit of claim 3, wherein said predetermined number of data of a series of instructions includes the instructions forming said series of instructions.

8. The circuit of claim 3, wherein said predetermined number of data of a series of

instructions includes the duration necessary to execute said series of instructions.

9. The circuit of any of claim 4, wherein the first means include, for each area of the memory, a predetermined number of registers.

10. The circuit of claim 9, wherein said predetermined number of registers includes index registers for managing the writing and the reading of the other registers of said predetermined number of registers, respectively by the fourth and second means.

11. The circuit of any of claim 5, wherein the first means include, for each area of the memory, a predetermined number of registers.

12. The circuit of claim 11, wherein said predetermined number of registers includes index registers for managing the writing and the reading of the other registers of said predetermined number of registers, respectively by the fourth and second means.

13. The circuit of any of claim 6, wherein the first means include, for each area of the memory, a predetermined number of registers.

14. The circuit of claim 13, wherein said predetermined number of registers includes index registers for managing the writing and the reading of the other registers of said predetermined number of registers, respectively by the fourth and second means.

15. The circuit of any of claim 7, wherein the first means include, for each area of the memory, a predetermined number of registers.

16. The circuit of claim 15, wherein said predetermined number of registers includes index registers for managing the writing and the reading of the other registers of said predetermined number of registers, respectively by the fourth and second means.

17. The circuit of any of claim 8, wherein the first means include, for each area of the memory, a predetermined number of registers.

18. The circuit of claim 17, wherein said predetermined number of registers includes index registers for managing the writing and the reading of the other registers of said predetermined number of registers, respectively by the fourth and second means.